Design and Analysis of Two-Stage CMOS Op-Amp with the Effect of Scaling-Review

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ABSTRACT:
This paper presents to design a two stage CMOS operational amplifier and analyze the effect of various aspect ratios on the characteristics of this op-amp, which operates at 1V power supply and using 32nm, 45nm, 90nm, 130nm, 180nm technology. In this paper trade-off curves are computed between all characteristics such as Gain, PM, O/P Swing, Slew Rate. The op-amp designed is a two-stage CMOS op-amp. Design has been carried out in tanner tools. The task of CMOS operational amplifiers (op-amps) design optimization is investigated in this work. This paper focuses on the optimization of different aspect ratio, which gives the results of the different parameters. When the task is analyzed as a search problem, it can be converted into an operational amplifier in which a variety of specifications, the Gain, PM, and other multi-objective optimization application. As a result, with respect to the operational amplifier having a standard feature helps graphics and tables under comparison. The simulation results agree with the theoretical predictions.

Keywords: CMOS Analog circuit, Two-Stage CMOS Operational Amplifier, Scaling, Tanner, 32nm, 45nm, 90nm, 130nm, 180nm.

I. INTRODUCTION

In the past few years, the electronics industry has exploded. The largest portion of total global sales market is dominated by the MOS. CMOS technology has been continuously and the minimum feature size of maturation. Design is becoming a high performance analog ICs for reducing the supply voltage and the transistor channel length relentless trend increasingly urgent. MOS transistor successful large part due to the fact that it can be extended to smaller and smaller dimensions which results in higher performance. Individual transistor feature size is reduced from deep summing micron (DSM) to even nano meter area. As the scale of integration increase more transistors, faster, smaller than their predecessors is packaged into a single chip. This has led to steady growth in operating frequency and each chip processing power. [7]

Operational Amplifier is the most common building blocks of most electronic systems may need no introduction. Operational Amplifier continues as a power supply voltage, the transistor channel length scaled down to each generation of CMOS technology challenge. In a different aspect ratio, there is a tradeoff between speed, power, gain, and other performance parameters. A CMOS op amp that combines high-gain frequency corresponding to DC gain of implementation has been a problem. This question has been evading a circuit of several methods. [5]

Purpose design method in this paper is to present a simple, yet accurate equation, 2 high-gain designs staged CMOS operational amplifier. To do this, some meaningful parameters (phase margin, gain bandwidth, etc.), a simple analysis. The method for processing a very wide variety of specifications and constraints. In this paper, we develop CMOS op amp design issues and their aspect ratio. Our proposed method can be applied to a wide variety of amplifier structure, but the application of the methods described herein specific CMOS operational amplifier. [6]

II. Design of Two-Stage CMOS op-amp

Many operational amplifier analog circuit design backbone. Op amp is a basic and important circuits widely used in analog circuits, such as speed switched-capacitor filter, algorithms, pipes and Σ-Δ A / D conversion, sample and hold amplifiers[2]. These circuits and accuracy depends on the one operational amplifier bandwidth and the DC gain. Bandwidth and greater accuracy and higher-speed operational amplifier is sampled data in analog circuits, such as a SC filter amplifier, a key factor of the modulator. Having a general block diagram of an output buffer of an operational amplifier is shown below. [3]
Figure 1: Block Diagram of Op-amp [1]

The first block is a differential amplifier. It has two inputs which are inverting and non-inverting voltage. It provides a differential voltage or differential current output terminal, basically, only dependent on the differential input. The next block is a differential-to-single-ended converter. It is used by the first group to generate the differential signal into a single-ended version. Some architecture does not require a single-ended to differential function so that the blocks can be excluded. In most cases, the gain provided by the input level is not enough, the need for additional amplification. This is accomplished by the intermediate stage, which is another of the differential amplifier, the first stage through the output driver provided. As the differential input stage uses the unbalanced output of the differential amplifier, it provides additional gain required. [3]

The first aspect considered in the design was the specification to be met. They appear in Table 1

<table>
<thead>
<tr>
<th>Specification Names</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply VDD</td>
<td>1.0V</td>
</tr>
<tr>
<td>Gain</td>
<td>70Db</td>
</tr>
<tr>
<td>Gain Bandwidth</td>
<td>10MHz</td>
</tr>
<tr>
<td>Settling Time</td>
<td>1u Sec</td>
</tr>
<tr>
<td>Slew Rate</td>
<td>10V/μSec</td>
</tr>
<tr>
<td>Input Common Mode Range</td>
<td>1.5-2.8V</td>
</tr>
<tr>
<td>Common Mode Rejection Ratio</td>
<td>60Db</td>
</tr>
<tr>
<td>Output Swing</td>
<td>1-2.8V</td>
</tr>
<tr>
<td>Offset</td>
<td>10m</td>
</tr>
</tbody>
</table>

A. Design methodology of op-amp[2]

Determine the necessary open-loop gain (Ao):

\[
\text{Drain Current } ID = \frac{\mu_n \cdot p \cdot \cos \left(\frac{W}{L}\right) \cdot V_{eff}^2}{2} \]

(1)

Gain margin \( g_m \) = \( 2\mu_n \cdot p \cdot \cos \left(\frac{W}{L}\right) \cdot Id \)

(2)

Gain margin \( g_m \) = \( 2 \cdot \frac{Id}{V_{eff}} \)

(3)

Slew rate \( SR = \frac{I_s}{C_{cc}} \)

(4)

First stage gain \( A_{v1} = \frac{-g_{m1}}{g_{ds2} + g_{ds4}} = \frac{-2g_{m1}}{I_s(A_{+}A_{-})} \)

(5)

Second stage gain \( A_{v2} = \frac{-g_{m1}}{g_{ds6} + g_{ds7}} = \frac{-2g_{m1}}{I_s(A_{+}A_{-})} \)

(6)

Gain Bandwidth \( GB = \frac{g_{m1}}{C_{cc}} \)

(7)

Output pole \( \rho_2 = \frac{-g_{m6}}{C_{L}} \)

(8)

RHP zero \( Z_1 = \frac{-g_{m6}}{C_{cc}} \)

(9)

Positive CMR \( V_{in}(\text{max}) = V_{DD} - \sqrt{\frac{I_s}{\beta_3}} - |V_{T03}(\text{max})| + V_{T1(\text{min})} \)

(10)

Negative CMR \( V_{in}(\text{min}) = V_{SS} + \sqrt{\frac{I_s}{\beta_1}} + V_{T1(\text{max})} + V_{DSS(sat)} \)

(11)
It is assumed that all transistors are in saturation for the above relationships. In this paper a two-stage op-amp with an n-channel input pair is designed. The op-amp uses a dual polarity power supply (VDD and VSS) for ac signal can swing above and below ground and also be centered at ground.

The calculation results provided the estimated parameters to make the circuit schematic shown in figure.

Figure 2: Schematic design of Two-Stage CMOS Op-Amp [6]

III. Implementation and SIMULATION

To analyze the behavior of variation in aspect ratios, first discuss the results of basic design of two stage CMOS Op-Amp.

A. AC Analysis

In AC-Analysis we determine Phase margin, Gain and GB OF THE Op-Amp.

Figure 3: Output of AC Analysis (32nm)  
Figure 4: Output of AC Analysis (45nm)

Figure 5: Output of AC Analysis (90nm)  
Figure 6: Output of AC Analysis (130nm)
B. DC Analysis:

Figure 7: Output of DC Analysis (32nm)

Figure 8: Output of DC Analysis (45nm)

Figure 9: Output of DC Analysis (90nm)

Figure 10: Output of DC Analysis (130nm)

C. Transient Analysis:

Figure 11: Transient pulse Analysis (32nm)

Figure 12: Transient pulse Analysis (45nm)
Table: 2 Comparison between different technologies

<table>
<thead>
<tr>
<th>Technology</th>
<th>180nm</th>
<th>130nm</th>
<th>90nm</th>
<th>45nm</th>
<th>32nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>PM</td>
<td>18°</td>
<td>23°</td>
<td>32°</td>
<td>62°</td>
<td>79°</td>
</tr>
<tr>
<td>GAIN(dB)</td>
<td>37</td>
<td>28</td>
<td>23</td>
<td>12.9</td>
<td>5.86</td>
</tr>
<tr>
<td>Slew Rate(V/us)</td>
<td>14.1</td>
<td>14.02</td>
<td>13.83</td>
<td>10.95</td>
<td>6.8</td>
</tr>
<tr>
<td>O/P Swing(V)</td>
<td>0.944</td>
<td>0.911</td>
<td>0.88</td>
<td>0.728</td>
<td>0.54</td>
</tr>
</tbody>
</table>

Table 3: Values of W of reference circuit (L= 45nm)

<table>
<thead>
<tr>
<th>W/L Ratio</th>
<th>Values (nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>W1,W2</td>
<td>67</td>
</tr>
<tr>
<td>W3,W4</td>
<td>333</td>
</tr>
<tr>
<td>W5</td>
<td>2094</td>
</tr>
<tr>
<td>W6</td>
<td>311</td>
</tr>
<tr>
<td>W7,W8</td>
<td>100</td>
</tr>
</tbody>
</table>

IV. CONCLUSIONS

This paper has presented the design, simulation and measurement consideration CMOS op-amps. The general approach to designing op-amps concentrates first on establishing dc conditions that are process insensitive. This result in defining some of the ration of the devices and establishing constraints between the device ratios. one important aspects of the op-amp is its stability characteristics, which are specified by the phase margin. Several compensation procedures that allow the designer to achieve reasonable good phase margins even with large capacitive loads were discussed. This paper has presented the principles and procedures by which the reader can design op-amps for application not requiring low output resistance.

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REFERENCES


